4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,138	12/03/2003	Kaushik Saha	852463.406	5322

38106 7590 07/11/2007

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 5400
SEATTLE, WA 98104-7092

EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
07/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,138	SAHA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/03/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 04/26/2007.

2. Claims 1-20 are pending in this application. Claims 1, 3, 5, and 16 are independent claims. In Amendment, claims 7-20 are added. This Office Action is made non-final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the radix-size within stages limitations within claims 8-9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8-9, 13-14, and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claim 8, the limitation "N minus two stages" in line 2 was not described in the specification in such a way as to reasably convey to one skilled in the relevant art that the inventor had possession of the claimed invention.

Re claim 9, the limitation "first plurality of stages comprises N stages" in lines 1-2 was not described in the specification in such a way as to reasably convey to one skilled in the relevant art that the inventor had possession of the claimed invention.

Re claims 13, 14, and 19, they have the same rejection as cited above.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-20 cite a FFT/IFFT in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-20 merely disclose steps/components for performing FFT/IFFT without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-20 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abel et al. (U.S. 5,991,787) in view of Jaber (U.S. 6,792,441).

Re claim 1, Abel et al. disclose in Figures 1-14 a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) using a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT).

Abel et al. fail to disclose in Figures 1-14 the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. However, Jaber discloses in Figures 8-9 the multiprocessing system (e.g. Figure 8 or Figure 9 as multiprocessing system for FFT/IFFT) for distributing the plurality of butterfly

operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage (e.g. abstract and col. 3 lines 30-68 wherein the input data is breakdown in block corresponding to each processor for computing Fourier Transform).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiprocessing system for distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and simultaneously (e.g. abstract and summary of the invention in cols. 3-4).

Re claim 2, Abel et al. fail to disclose in Figures 1-14 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor. However, Jaber discloses in Figures 8-9 step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor (e.g. col. 7 lines 2-30).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system

respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 3, it is a system claim of claim 1. Thus, claim 3 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 4, it is a system claim of claim 2. Thus, claim 4 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 5, it is a program product claim of claim 8. Thus, claim 5 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 6, it has similar limitations cited in claim 2. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 7, Abel et al. further disclose in Figures 1-14 the first radix is a radix-2 radix (e.g. component 800 in Figure 8 wherein the component 800 utilizes radix-2 to compute the butterfly computation of IFFT).

Re claim 8, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises N minus two stages (e.g. as $(\log_2 N) - 2$ stages are seen in component 800 in Figure 8), further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation (e.g. component 900 in Figure 9).

Re claim 9, Abel et al. further disclose in Figures 1-14 the first plurality of stages comprises N stages (e.g. Figure 4 and Figure 8).

Re claim 10, Abel et al. further disclose in Figures 1-14 an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT (e.g. output of Figure 4 or Figure 8).

Re claim 11, Abel et al. fail to disclose in Figures 1-14 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location. However, Jaber discloses in Figures 8-9 the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location (e.g. col. 15 lines 4-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location as seen in Jaber's invention into Abel et al.'s invention because it would enable to speed up the computation by computing in parallel and independent from each other (e.g. abstract and col. 6 line 60 to col. 7 line 30).

Re claim 12, it is a system claim of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, it is a system claim of claim 8. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 14, it is a system claim of claim 9. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 15, it is a system claim of claim 11. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 16, it is a computer-readable memory claim of claim 1. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a computer-readable memory claim of claim 2. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a computer-readable memory claim of claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 19, it is a computer-readable memory claim of claim 9. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it is a computer-readable memory claim of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Response to Amendment

9. The amendment filed 04/26/2007 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Re claims 8 and 13, the limitation "N minus two stages" is not found/supported in the original specification.

Re claims 9, 14, and 19, the limitation "the first plurality of stages comprises N stages" is not found/supported in the original specification.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

10. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,831,883 to Suter et al. disclose a low energy consumption, high performance Fast Fourier Transform.

U.S. Patent No. 5,313,413 to Bhatia et al. disclose an apparatus and method for preventing I/O bandwidth limitations in Fast Fourier Transform processors.

U.S. Patent No. 4,547,862 to McIver et al. disclose a monolithic Fast Fourier Transform circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 3, 2007